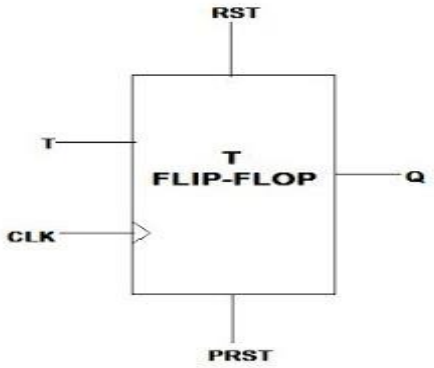
Course Title: **Digital Systems**	Course Code: **CCE2107**	Year: 2nd Computers
Date: **Nov. 22nd2014 (First term)**	Allowed time: **1:15 hr**	No. of Pages: (1)

Exam solution

1- Consider the block diagram of a T flip-flop shown in the figure, write the appropriate VHDL code describes its function.

(3 degrees)




```
libraryieee;
useieee. std_logic_1164.all;
useieee. std_logic_arith.all;
useieee. std_logic_unsigned.all;

entity T-FF is

PORT( T,CLK,PRST,RST: in std_logic;
                Q: out std_logic);

end T-FF;

architecture behavioral of T-FF is
begin

P1: process(CLK,PRST,RST)
variable x: std_logic;

begin
   if(RST='0') then
          x:='0';
  elsif(RST='1' and PRST='0') then
         x:='1';
  elsif(CLK='1' and CLK'EVENT) then
         if(T='1')then
                x:= not x;
        end if;
  end if;

  Q<=x;
end process;
end behavioral;
```

Q2) **State whether the following statements are correct or not, if not state the correct**

a. It is possible to check previous values of VHDL signals.

True

b. Declaration of an internal signal contains the name of the signal, its mode and type.

False

c. All signals of a system are defined in the system's entity.

False **(3 degrees)**

Q3) **Write the appropriate VHDL statement for the following operations:**

a) Define a new data type with a name small_int and the values 1,2,3,4.

Type small_int is ('1','2','3','4');

b) Shift left the value of the signal Num into two positions.

Numsll 2;

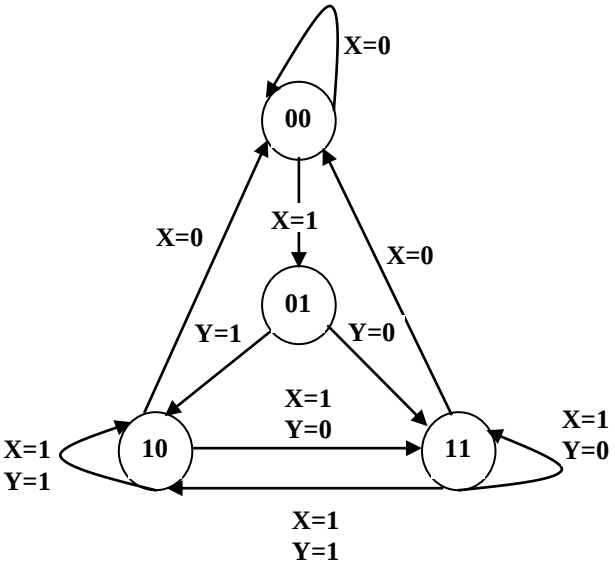
c) A statement waits for an event on signals load and ready and continues only if load and ready is true at the time of the event, or until10nsec of time has elapsed.

wait on load, ready until (load=true and ready=true) for 10 ns;

(3 degrees)

Q4: Design the sequential circuit which behaves as shown in the following state diagram using D flip-flop (no need to draw if there is no time).

(5 degrees)



Present State		Inputs		Next State = D FF inputs	
A1	A0	X	Y	A1+ (D1)	A0+ (D0)
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	1	1
0	1	0	1	1	0
0	1	1	0	1	1
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	1	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	1	1
1	1	1	1	1	0

Simplifying D1 = A1'. A0 + A1. X

D0 = X.Y + A1'.A0'.X + A1'.A0.Y'

Q5: For the given state table for a Mealy machine, reduce to a minimum number of states and find a "good" state assignment.

(3 degrees)

Present state	Next state (x=0)	Next state (x=1)
a	b/0	c/0
b	d/0	e/0
c	e/0	a/0
d	d/0	e/0
e	c/0	a/0

We can see that b = d, so we will omit the d raw, and replace each d with a b in the table to give the following table.

Present state	Next state (x=0)	Next state (x=1)
a	**b/0**	**c/0**
b	**b/0**	**e/0**
c	**e/0**	**a/0**
e	**c/0**	**a/0**

The assignment is:

a = 00, b = 01, c = 10 and e = 11

<u>Q6:</u> What is the difference between the J-K flip flop and D flip flop in their response to the inputs? Which of them is preferred in the design and why? (<u>3 degrees</u>)

J	K	Response
0	**0**	**No change**
0	**1**	**Reset**
1	**0**	**Set**
1	**1**	**Complement**

Q(t+1) = D

We prefer to use JK as it produces less complicated circuit which contains less gates and thus less power, size and effort.